

ABSTRACT

Management of accessing data in a main memory and a cache memory includes, for each unit of data transferred from a first processor to a second processor, filling a cache set of the cache memory with data associated with addresses in the main memory that correspond to the cache set after the first processor writes a unit of data to addresses that correspond to the cache set. For each unit of data transferred from the second processor to the first processor, filling the cache set with data associated with addresses in the main memory that correspond to the cache set before the first processor reads a unit of data written by the second processor to addresses that correspond to the cache set. The data used to fill the cache set are associated with addresses that are different from the addresses associated with the unit of data.

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